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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/507,825	02/22/2000	Shunpei Yamazaki	SEL 162	2841

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EXAMINER
LEWIS, DAVID LEE

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/507,825	Yamazaki et al.
Examiner	**Art Unit**
David L. Lewis	2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Sep 17, 2002*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-80* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-80* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Title: Display Device

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

2. **Claims 1-4, 11-14, 21-24, 31-34, 41-44, 51-54, 61-64, and 71-74 are rejected under 35 U.S.C. 102(e) as being anticipated by Kubota et al. (6067066).**

3. **As in claim 1, Kubota et al. teaches** of a display device comprising: a pixel region with a plurality of pixel TFTs arranged in matrix, **figure 2**; and at least one source driver and at least one gate driver for driving said pixel region, **figure 2 items 2 and 3**, wherein of m bit digital video data inputted from the external. upper n bit data and lower (m - n) bit data are used as gradation voltage information and time gradation information, respectively, where m and n are both positive integers equal to or larger than 2 and satisfy m > n, **figures 1, 14, or 24, column 23 lines 15-53**.

4. **As in claim 11, Kubota et al. teaches** of a display device comprising: a pixel region with a plurality of pixel TFTs arranged in matrix, **figure 2**; at least one source driver and at least one gate driver for driving said pixel region, **figure 2 items 2 and 3**, and a circuit for converting m bit digital video data inputted from the external into n bit digital video data for gradation voltage, and for supplying said source driver with said n bit digital video data (m and n are both positive integers equal to or larger than 2, in > n). wherein one frame of image consists of 2m-n sub-frames to perform time gradation display, **figures 1, 14, or 24, column 23 lines 15-53**.

5. **As in claim 21, Kubota et al. teaches** of a display device comprising: a pixel region with a plurality of pixel TFTs arranged in matrix, **figure 2**; at least one source driver and at least one gate driver for driving said pixel region, **figure 2 items 2 and 3**, and a circuit for converting m bit digital video data inputted from the external into n bit digital video data for gradation voltage and for supplying said source driver with said n bit digital video data (m and n are both positive integers equal to or larger than 2. in > n). wherein one frame of image consists of 2m-n sub-frames to perform time gradation display, thereby obtaining (2m - (2m-n - 1)) patterns of gradation display, **figures 1, 14, or 24, column 23 lines 15-67**.

6. **As in claim 31, Kubota et al. teaches** of a display device comprising a pixel region with a plurality of pixel TFTs arranged in matrix and at least one source driver and at least one gate driver for driving

said pixel region, **figure 2 items 2 and 3**, wherein of m bit digital video data inputted from the external. upper n bit data and lower (m - n)bit data are used as gradation voltage information and time gradation information, respectively (m and n are both positive integers equal to or larger than 2. m > n), **figures 1, 14, or 24, column 23 lines 15-53**, and wherein said source driver has a D/A converter circuit for converting said n bit digital video data into analog gradation voltage, **figure 1 and 14 items 17 and 18, figure 24 item 15, wherein digital decoding and analog switching combine to form said D/A converter**.

7. **As in claim 41, Kubota et al. teaches** of a display device comprising: a pixel region with a plurality of pixel TFTs arranged in matrix, **figure 2**; at least one source driver and at least one gate driver for driving said pixel region, **figure 2 items 2 and 3**; and a circuit for converting m bit digital video data inputted from the external into n bit digital video data for gradation voltage, and for supplying said source driver with said n bit digital video data (m and n are both positive integers equal to or larger than 2, m > n), **figures 1, 14, or 24, column 23 lines 15-53**, wherein said source driver has a D/A converter circuit for converting said n bit digital video data into analog gradation voltage, **figure 1 and 14 items 17 and 18, figure 24 item 15, wherein digital decoding and analog switching combine to form said D/A converter**, and wherein one frame of image consists of 2m-n sub-frames to perform time gradation display, **column 25 lines 15-28.**

8. **As in claim 51, Kubota et al. teaches** of a display device comprising: a pixel region with a plurality of pixel TFTs arranged in matrix, **figure 2**, at least one source driver and at least one gate driver for driving said pixel region, **figure 2 items 2 and 3**, and a circuit for converting m bit digital video data inputted from the external into n bit digital video data for gradation voltage, and for supplying said source driver with said n bit digital video data (m and n are both positive integers equal to or larger than 2. in > n), **figures 1, 14, or 24, column 23 lines 15-53**, wherein said source driver has a D/A converter circuit for converting said n bit digital video data into analog gradation voltage, **figure 1 and 14 items 17 and 18, figure 24 item 15, wherein digital decoding and analog switching combine to form said D/A converter**, and wherein one frame of image consists of 2m-n sub-frames to perform time gradation display, thereby obtaining (2'm - (2m-n - 1)) patterns of gradation display, **column 25 lines 15-67**.

9. **As in claim 61, Kubota et al. teaches** of a display device comprising: a pixel region with a plurality of pixel TFTs arranged in matrix, **figure 2,** at least one source driver and at least one gate driver for driving said pixel region, **figure 2 items 2 and 3**; a circuit for converting m bit digital video data inputted from the external into n bit digital video data for gradation voltage (m and n are both positive integers equal to or larger than 2, m > n), **figures 1, 14, or 24, column 23 lines 15-53**; and a D/A converter circuit for converting said n bit digital video data into analog video data to input the

converted data to said source driver, **figure 1 and 14 items 17 and 18, figure 24 item 15, wherein digital decoding and analog switching combine to form said D/A converter**, wherein one frame of image consists of 2m-n sub-frames to perform time gradation display, **column 25 lines 15-28**.

10. **As in claim 71, Kubota et al. teaches** of a display device comprising: a pixel region with a plurality of pixel TFTs arranged in matrix, **figure 2**; at least one source driver and at least one gate driver for driving said pixel region, **figure 2 items 2 and 3**; a circuit for converting m bit digital video data inputted from the external into n bit digital video data for gradation voltage (m and n are both positive integers equal to or larger than 2, m > n), **figures 1, 14, or 24, column 23 lines 15-53**; and a D/A converter circuit for converting said n bit digital video data into analog video data to input the converted data to said source driver, **figure 1 and 14 items 17 and 18, figure 24 item 15, wherein digital decoding and analog switching combine to form said D/A converter**, wherein one frame of image consists of 2m-n sub-frames to perform time gradation display, thereby obtaining (2m - (2m-n - 1)) patterns of gradation display, **column 25 lines 15-67**.

11. **As in claims 2, 3, 12, 13, 22, 23, 32, 33, 42, 43, 52, 53, 62, 63, 72, and 73 Kubota et al.** teaches of wherein said m is 8/12 and said n is 2/4, column 23 lines 15-53, wherein m and n are integers covering said values. **As in claims 4, 14, 24, 34, 44, 54, 64, and 74, Kubota et al.** teaches of wherein said display device is a liquid crystal display device, column 19 lines 60-62.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 5-10, 15-20, 25-30, 35-40, 45-50, 55-60, 65-70, and 75-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. (6067066) in view of Takano et al. (6165824) and Hasegawa et al. (6335717).**

14. **As in claims 5-10, 15-20, 25-30, 35-40, 45-50, 55-60, 65-70, and 75-80, Kubota et al.** teaches of the invention as applied above to claims 1, 11, 21, 31, 41, 51, 61, and 71, however Kubota is silent as to said various display types. Said display types of claims 5-10, 15-20, 25-30, 35-40, 45-50, 55-60, 65-70, and 75-80 represent display systems well known in the art of displays, any of which would have been obvious to the skilled artisan at the time of the invention of Kubota et al. to implement them in a display system as taught by **Kubota et al.**, given that such an active matrix type display system as taught by Kubota et al. is well known in incorporated in each of said display types. In

support of said display types being obviously well **known both Takano et al., figures 12A-F, and Hasegawa et al., column 1 lines 7-45**, teaches of said various display types as well known in the art of displays, as found in claims 5-10, 15-20, 25-30, 35-40, 45-50, 55-60, 65-70, and 75-80.

Response to Arguments

15. Applicant's arguments filed 9/17/2002 have been fully considered but they are not persuasive. Kubota et al. teaches of n bit input data, wherein gradation voltage and time gradation are both used. As shown on column 22 lines 27-67, column 23 lines 15-67, and column 25 lines 29-51, Kubota teaches first n-bit digital signal is sampled by the sampling circuit 12, and thereafter divided into m-bit and k-bit data, over a period of 2k, wherein one of the gradation voltages with a level of 2(m+k) is outputted. For example, in the case where a 6 bit digital signal is divided into m-3 bits and k=3 bits, 64 gradation display is possible by 8 gradation power source lines during the horizontal scanning period. When one analog switch in the output switches 18 conducts according to the 2m writing pulses S during a period where the period selecting signal PRD is ON, one of the 2m gradation power source lines PL is selected. As a result, a desired gradation voltage is outputted t the source line SL during one period of the 2k periods. Rejection maintained.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. **6232941, 6459416, 6320565, 6462728, 6239781, 6452583, 6229583.**

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(703) 306-3026**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on (703) 305-4938. Any

inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231
or faxed to:
(703) 872-9314 (for Technology Center 2600 only)
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600